

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently Amended) An apparatus for routing data between
2 integrated circuit devices, comprising:
3 an ~~n-dimensional~~ two-dimensional grid of integrated circuit devices;
4 a plurality of communication networks coupling the ~~n-dimensional~~ two-
5 dimensional grid of integrated circuit devices, ~~wherein a communication network~~
6 ~~of the plurality of communication networks moves data unidirectionally in only~~
7 ~~orthogonal dimensions~~ wherein the plurality of communication networks includes:
8 a first separate communication network configured to move data
9 unidirectionally in a North direction and an East direction along
10 communication lines used by only the first communication network;
11 a second separate communication network configured to move data
12 unidirectionally in the North direction and a West direction along
13 communication lines used by only the second communication network;
14 a third separate communication network configured to move data
15 unidirectionally in a South direction and the East direction along
16 communication lines used by only the third communication network; and
17 a fourth separate communication network configured to move data
18 unidirectionally in the South direction and the West direction along
19 communication lines used by only the fourth communication network; and

20 a routing mechanism configured to route data across the plurality of
21 communication networks as well as into, out of, and through a given integrated
22 circuit within the ~~n-dimensional~~ two-dimensional grid of integrated circuits;
23 whereby a process of routing ~~signals~~ data across a given communication
24 network is greatly simplified because it is not possible to create a cycle that causes
25 a deadlock within the given communication network; and
26 whereby the process of routing ~~signals~~ data yields a shortest path between
27 source and destination.

1 2. (Original) The apparatus of claim 1, wherein the n-dimensional
2 grid of integrated circuit devices includes memory devices.

1 3. (Original) The apparatus of claim 1, wherein the n-dimensional
2 grid of integrated circuit devices includes processor devices, I/O devices, digital
3 signal processors, field programmable gate arrays, sensors, and controllers.

1 4. (Cancelled)

1 5. (Original) The apparatus of claim 1, wherein the routing
2 mechanism is configured to statically route data items across the plurality of
3 communication networks.

1 6. (Original) The apparatus of claim 1, wherein the routing
2 mechanism is configured to dynamically route data items through network
3 junctions within each integrated circuit.

1 7. (Original) The apparatus of claim 1,

2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and
5 wherein during a dynamic routing process, the routing mechanism
6 removes a horizontal step or a vertical step from the header for the data item,
7 depending upon which direction is dynamically selected.

1 8. (Currently Amended) A method for creating a computing system,
2 comprising:

3 creating ~~an n-dimensional~~ a two-dimensional grid of integrated circuit
4 devices;

5 establishing a plurality of communication networks coupling the ~~n-~~
6 ~~dimensional~~ two-dimensional grid of integrated circuit devices, ~~wherein a~~
7 ~~communication network of the plurality of communication networks moves data~~
8 ~~unidirectionally in only orthogonal dimensions,~~ wherein establishing the plurality
9 of communication networks involves;

10 establishing a first separate communication network configured to
11 move data unidirectionally in a North direction and an East direction along
12 communication lines used by only the first communication network;

13 establishing a second separate communication network configured
14 to move data unidirectionally in the North direction and a West direction
15 along communication lines used by only the second communication
16 network;

17 establishing a third separate communication network configured to
18 move data unidirectionally in a South direction and the East direction
19 along communication lines used by only the third communication network;
20 and

21 establishing a fourth separate communication network configured
22 to move data unidirectionally in the South direction and the West direction
23 along communication lines used by only the fourth communication
24 network; and
25 providing a routing mechanism configured to route data across the
26 plurality of communication networks as well as into, out of, and through a given
27 integrated circuit within the ~~n-dimensional~~ two-dimensional grid of integrated
28 circuits;
29 whereby a process of routing ~~signals~~ data across a given communication
30 network is greatly simplified because it is not possible to create a cycle that causes
31 a deadlock within the given communication network; and
32 whereby the process of routing ~~signals~~ data yields a shortest path between
33 source and destination.

1 9. (Original) The method of claim 8, wherein the n-dimensional grid
2 of integrated circuit devices includes memory devices.

1 10. (Original) The method of claim 8, wherein the n-dimensional grid
2 of integrated circuit devices includes processor devices, I/O devices, digital signal
3 processors, field programmable gate arrays, sensors, and controllers.

1 11. (Cancelled)

1 12. (Original) The method of claim 8, wherein the routing mechanism
2 is configured to statically route data items across the plurality of communication
3 networks.

1 13. (Original) The method of claim 8, wherein the routing mechanism
2 is configured to dynamically route data items through network junctions within
3 each integrated circuit.

1 14. (Original) The method of claim 8,
2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and
5 wherein during a dynamic routing process, the routing mechanism
6 removes a horizontal step or a vertical step from the header for the data item,
7 depending upon which direction is dynamically selected.

1 15. (Currently Amended) A means for routing data between integrated
2 circuit devices within ~~an n-dimensional~~ a two-dimensional grid of integrated
3 circuit devices, comprising:
4 a communication means comprising a plurality of communication
5 networks coupling the ~~n-dimensional~~ two-dimensional grid of integrated circuit
6 devices, wherein ~~a communication network of the plurality of communication~~
7 ~~networks moves data unidirectionally in only orthogonal dimensions~~
8 a first separate communication network moves data
9 unidirectionally in a North direction and an East direction along
10 communication lines used by only the first communication network;
11 a second separate communication network moves data
12 unidirectionally in the North direction and a West direction along
13 communication lines used by only the second communication network;
14 a third separate communication network moves data
15 unidirectionally in a South direction and the East direction along
16 communication lines used by only the third communication network; and

17 a fourth separate communication network moves data
18 unidirectionally in the South direction and the West direction along
19 communication lines used by only the fourth communication network; and
20 a routing means for routing data across the plurality of communication
21 networks as well as into, out of, and through a given integrated circuit within the
22 ~~n-dimensional~~ two-dimensional grid of integrated circuits;
23 whereby the means of routing ~~signals~~ data yields a shortest path between
24 source and destination.

1 16. (Original) The means of claim 15, wherein the n-dimensional grid
2 of integrated circuit devices includes memory devices.

1 17. (Original) The means of claim 15, wherein the n-dimensional grid
2 of integrated circuit devices includes processor devices, I/O devices, digital signal
3 processors, field programmable gate arrays, sensors, and controllers.

1 18. (Cancelled)

1 19. (Original) The means of claim 15, wherein data is configured to
2 statically routed across the plurality of communication networks.

1 20. (Original) The means of claim 15, wherein data is dynamically
2 routed through network junctions within each integrated circuit.

1 21. (Original) The means of claim 15,
2 wherein a header attached to each data item in a two-dimensional grid
3 indicates a number of horizontal steps and a number of vertical steps required for
4 the data item to reach its destination; and

5 wherein during a dynamic routing process, a horizontal step or a vertical
6 step is removed from the header for the data item, depending upon which
7 direction is dynamically selected.